XRM2-CLINK-GIGE User Manual

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1 Introduction

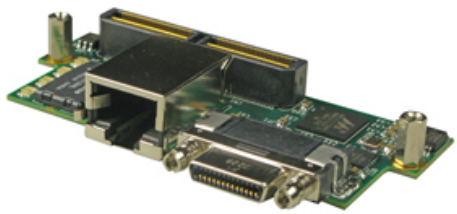

Figure 1: XRM-CLINK-GIGE Photo

The XRM-CLINK-GIGE provides a RGMII 1000/100/10 Ethernet PHY, RS232 transceiver, and mini Cameralink interfaces for the Alpha Data's FPGA based platforms.

The XRM-CLINK-GIGE is designed to allow the deployment of systems that require Gigabit Ethernet capability (for example GigE-Cameralink) and mini Cameralink connectivity.

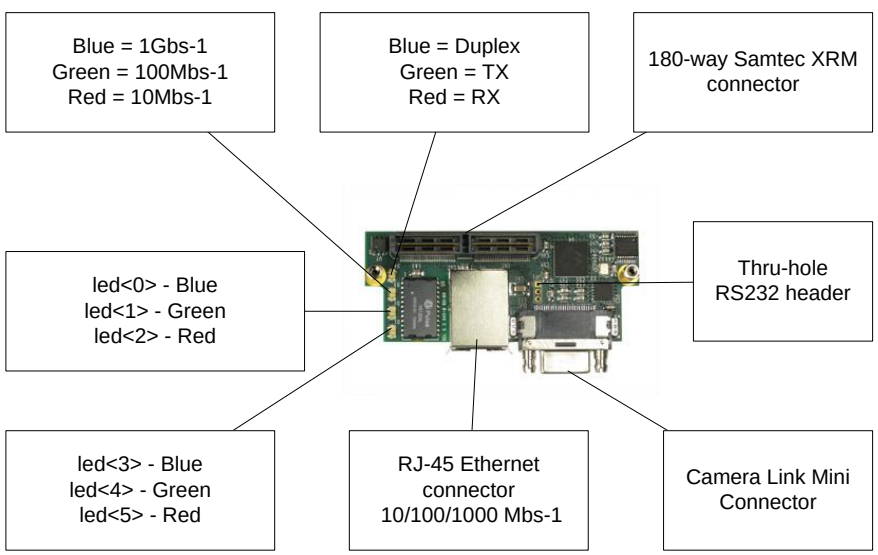

Figure 2: XRM-CLINK-GIGE Features

2 Installation

The XRM-CLINK-GIGE is designed to plug in to the front panel connector (SAMTEC QSH series) on the FPGA base card. The retaining screws should be tightened to secure the XRM-CLINK-GIGE.

If using a ADM-XRC-5 series board or old ensure that the VIO voltage for the base FPGA card is set to 2.5V. Please refer to the base FPGA card's User Guide on setting the VIO voltage.

Note: This operation should not be performed while the host PMC/XMC or PCI card is powered up.

XRM IO voltage will automatically be set for ADM-XRC-6 series board and later.

2.1 Handling instructions

Observe precautions for preventing damage to components by electrostatic discharge. Personnel handling the board should take SSD precautions.

Avoid flexing the board.

3 Specification

3.1 Connectors

SDR connector 3M part number 12226-8250-00FR

Standard RJ-45 connector

3.2 Mating Cableform

3.2.1 SDR connector

SDR cable assembly 3M part number 1SF26-L120-00C-XXX, where XXX= length in centimetres.

SDR to MDR cable assembly 3M part number 1MF26-L560-00C-XXX, where XXX= length in centimetres.

3.2.2 RJ-45 connector

Standard RJ-45 Cat 5e/6 cable.

3.2.3 Miscellaneous

RS232 transceiver controlled from FPGA implementing 3-wire interface. Connection via 3-pin 1.0 mm thru-hole header.

3.3 Order Code

XRM-CLINK-GIGE

For further information please contact Alpha Data.

4 Related Documents

Camera Link Specification v1.1 (Automated Imaging Association)

CameraLink Technology Brief Available from http://www.baslerweb.com

Xilinx EDK documentation. http://www.xilinx.com/ise/embedded_design_prod/platform_studio.htm

5 Design Examples

Example UCF, HDL files and Application software are available from Alpha Data for for purchasers of this card.

6 Pinout

6.1 Samtec pinout

The pin numbers in the section should be used with the usermanual or SDK for a board it is being attached to to create a UCF. Example UCFs may also be available on request from support@alpha-data.com

Signal Name	Direction	Samtec pin	SDR pin (Con. 1)
xclk_p	in	102	9
xclk_n	in	104	22
x_p<0>	in	64	25
x_n<0>	in	62	12
x_p<1>	in	68	11
x_n<1>	in	66	24
x_p<2>	in	72	10
x_n<2>	in	70	23
x_p<3>	in	74	8
x_n<3>	in	76	21
cc_p<1>	out	88	5
cc_n<1>	out	86	18
cc_p<2>	out	83	17
cc_n<2>	out	81	4
cc_p<3>	out	100	3
cc_n<3>	out	98	16
cc_p<4>	out	87	15
cc_n<4>	out	85	2
ser_tfg_p	in	82	6
ser_tfg_n	in	84	19
ser_tc_p	out	80	20
ser_tc_n	out	78	7

Table 1: Camera Link Connector 1 (Base Configuration)

Signal Name	Direction	Samtec pin	Notes
led<0>	out	8	Blue
led<1>	out	14	Green
led<2>	out	16	Red
led<3>	out	73	Blue
led<4>	out	71	Green
led<5>	out	69	Red

Table 2: LED Indicators

Signal Name	Direction	Samtec pin	Notes
gige_mdio	inout	24	Management data
gige_mdc	out	36	Management data clock. Max. freq 8.3MHz
gige_reset_l	out	30	Active low reset
gige_clk125	in	89	125MHz clock source
gige_crs	in	27	Carrier sence
gige_col	in	35	Collision
gige_int_l	in	28	Active low interrupt
gige_tx_ctl	out	23	RGMII tx control
gige_txc	out	91	RGMII tx clock. 125MHz/25MHz/2.5MHz
gige_txd<0>	out	11	RGMII tx data
gige_txd<1>	out	19	
gige_txd<2>	out	7	
gige_txd<3>	out	3	
gige_rxd<0>	in	25	RGMII tx data
gige_rxd<1>	in	9	
gige_rxd<2>	in	21	
gige_rxd<3>	in	37	
gige_rx_ctl	in	13	RGMII rx control
gige_rxc	in	40	RGMII rx clock 125MHz/25MHz/2.5MHz

Table 3: RGMII PHY Interface

Signal Name	Direction	Samtec pin	Notes
tx	out	99	RS232 compatible output
rx	in	29	RS232 compatible input
force	out	105	Active high enable for RS232 interface
ready	in	22	Active high
invalid_l	in	97	Active low for framing error

Table 4: RS232 Interface

6.2 RS232 thru-hole header

Pin	Function	Direction
1	tx	out
2	gnd	n/a
3	rx	in

The tables below show the electrical characteristics of the RS232 connection under typical operating conditions.

RX Inputs	Min	Tpy	Max	Units
Input Voltage Range	-25		25	V
Input Threshold Low	0.6	1.2		V
Input Threshold High	n/a	1.5	2.4	V
Input Hysteresis	n/a	0.5		V
Input Resistance	3	5	7	kΩ

Table 5: RX input

TX Outputs	Min	Tpy	Max	Units
Output Voltage Swing	±5	n/a	±5.4	V
Output Resistance	300	n/a	10M	Ω
Output Short-Circuit Current	n/a	n/a	±60	mA
Output Leakage Current	n/a	n/a	±60	µA

Table 6: TX output

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Revision History:

Date	Revision	Nature of Change
Jul-2008	1.0	First release.
Oct-2008	1.1	Fixed mistakes in pin names and added PHY defaults.
April-2008	2.0	Updated document to reflect hardware changes to the XRM-Clink-GIGE.
Feb-2011	2.1	Updated document for XRC-6T1 support and conversion to XML document format.

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